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(54) **DISPLAY DEVICE, PDP DISPLAY DEVICE, AND ITS DRIVING CIRCUIT**

(57) Abstract:

PROBLEM TO BE SOLVED: To improve a switching characteristic by lightening the burn of a drive circuit of an output element and to reduce voltage drop at the time of conduction by using IGBT in which fast speed operation is performed as an output element of a driving circuit of a panel.

SOLUTION: IGBT is used for output elements 11a, 11b. IGBT is used for also switching elements 12a, 12b for recovering electric power. IGBT has a bad current cut off characteristic and especially a tail current appears remarkably, but defect of IGBT can be compensated by combining increase of operation speed of a current cut off characteristic of IGBT and Ac type PDP in which a charge current is stopped independently of that sustaining voltage is applied to an electrode. Thereby, as for voltage drop, further improvement can be performed by using IGBT of which voltage drop is small as an element (as compared with a power MOS FET of the same chip size) when a current is made to flow as output elements 11a, 11b.

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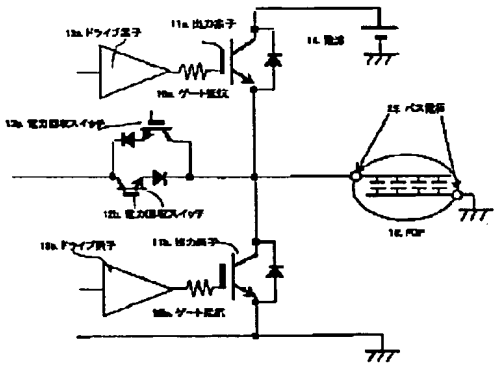

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(54) **IC FOR AC-TYPE PLASMA DISPLAY DRIVING**

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(57) Abstract:

PURPOSE: To prevent the parasitic effect and to reduce the chip area by forming an IC on a dielectric isolation semiconductor substrate (laminated SOI substrate).

CONSTITUTION: An IC is formed on a dielectric isolation semiconductor substrate. An SOI substrate, especially a lamination type SOI substrate 13 is used as the dielectric isolation semiconductor substrate. The lamination type SOI substrate 13 is formed by laminating a supporting substrate 14 and an n-drift layer 16 by a lamination oxide film 15. The thickness of the n-drift layer 16 is 15μm or more and 20μm or less and its resistivity is 5Ω.cm or more and 50Ω.cm or less. If the thickness of the lamination oxide film 15 is 0.5μm or more and 3μm or less, it is further effective. An element region is electrically isolated from the supporting substrate 14 and parasitic effect can be prevented by forming an IC on the lamination type SOI substrate 13 in this way. A chip area can be also reduced.